M.Tech.

IN

VLSI & EMBEDDED SYSTEM

CURRICULUM AND SYLLABUS

(Applicable from 2026 onwards)

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY MANIPUR

Langol Road, Lamphelpat, Imphal, Manipur - 795004

Semester I

Sl. No.	Course Code	Course Name	L	T	P	Credits
1.	VL 5101	Analog IC Design	3	1	0	4
2.	VL 5102	Embedded Systems Design	3	1	0	4
3.	VL 5103	Semiconductor Device Modelling	3	1	0	4
4.	VL 5104	VLSI System Design	3	0	0	3
5.	VL 5110	Seminar-I	0	0	4	2
6.	VL 515x	Elective-I	3	0	0	3
7.	VL 516x	Elective-II	0	0	6	3
		Total	15	3	10	23

Semester II

Sl. No.	Course Code	Course Name	L	T	P	Credits
1.	VL 5201	Digital CMOS IC Design	3	1	0	4
2.	VL 5202	Semiconductor IC Technology	3	1	0	4
3.	VL 5203	Low Power VLSI	3	1	0	4
4.	VL 5204	Real Time Operating System	3	0	0	3
5.	VL 5210	Seminar-II	0	0	4	2
6.	VL 525x	Elective-III	3	0	0	3
7.	VL 526x	Elective-IV	0	0	6	3
		Total	15	3	10	23

Semester III

Sl. No.	Course Code	Course Name	L	T	P	Credits
1.	VL 6301	Project-I	0	0	24	12
2.	VL 6310	Comprehensive-Viva	0	0	0	2
		Total	0	0	24	14

Semester IV

Sl. No.	Course Code	Course Name	L	T	P	Credits
1.	VL 6401	Project-II	0	0	40	20
		Total	0	0	40	20

List of Departmental Electives

Sl. No.	Course Code	Course Name	L	T	P	Credits	Category
1.	VL 5151	Digital System Design	3	0	0	3	Elective I
2.	VL 5152	Signal Processing for Embedded Systems	3	0	0	3	
3.	VL 5153	Microcontroller for Embedded Systems	3	0	0	3	
4.	VL 5154	Embedded Networking	3	0	0	3	
5.	VL 5155	FPGA Design	3	0	0	3	
6.	VL 5156	VLSI DSP	3	0	0	3	
7.	VL 5157	Digital IC Design	3	0	0	3	
8.	VL 5158	MEMS and Microsystem Technology	3	0	0	3	
9.	VL 5159	Biomedical Signal and Systems	3	0	0	3	
10.	VL 5261	VLSI and Embedded Lab-I	0	0	6	3	Elective II
11.	VL 5262	Signal and Image Processing Lab	0	0	6	3	
12.	VL 5251	ASIC Design and Modeling	3	0	0	3	Elective III
13.	VL 5252	Embedded Computing	3	0	0	3	
14.	VL 5253	VLSI EDA Tools	3	0	0	3	
15.	VL 5254	Reconfigurable Computing	3	0	0	3	
16.	VL 5255	Memory Technologies	3	0	0	3	
17.	VL 5255	Filter Design	3	0	0	3	
18.	VL 5255	CPLD & FPGA Architecture	3	0	0	3	
19.	VL 5256	System on Chip (SoC)	3	0	0	3	
20.	VL 5261	VLSI and Embedded Lab-II	0	0	6	3	Elective IV
21.	VL 5262	System Simulation Lab-A	0	0	6	3	

Course Code: VL 5101	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	Y	N
Type of Course	Theory		
Course Title	**Analog IC Design (VL 5101)**		
Course Objectives	• This course covers the analysis, design, and layout of CMOS analog integrated circuits. It bridges the gap between basic circuit theory and the complex trade-offs (speed, power, noise, and gain) required in modern silicon design. • Students will transition from single-transistor stages to complex systems like Operational Amplifiers and Bandgap References, with a strong emphasis on MOS device physics and parasitic effects.		

Course Outcomes		**Cognitive Levels**
CO1	Model MOSFETs accurately for high-frequency analog circuit simulations.	Knowledge/Comprehension (Level I/Level-II)
CO2	Analyze and design basic analog functional blocks like current mirrors and differential pairs.	Analysis (Level-IV)
CO3	Design a complete CMOS Operational Amplifier based on specific industrial requirements (gain, BW, power).	Application (Level-III)
CO4	Evaluate the stability of multi-stage amplifiers and apply appropriate compensation techniques.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**	**Summer**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	1	0	4	48
Prerequisite course codes with course names	**Introduction to Semiconductor Devices (EC2403), Analog Electronics (EC2303)**				

Text Books		
1.	Title	Design of Analog CMOS Integrated Circuits
	Author	Behzad Razavi
	Publisher	McGraw Hill.
	Edition	3rd Edition
2.	Title	CMOS Analog Circuit Design
	Author	P.E. Allen and D.R. Holberg
	Publisher	Oxford University Press
	Edition	2nd ed.

Reference Books		
1.	Title	CMOS Circuit Design, Layout, and Simulation
	Author	R. Jacob Baker
	Publisher	IEEE Press/Wiley

	Edition	5th edition	
Course Contents	**Unit 1**: **MOS Device Modeling & Single-Stage Amplifiers** Review of MOS Physics: I-V characteristics, second-order effects (Body effect, Channel length modulation, Sub-threshold conduction), Small-Signal Models: High-frequency models and parasitic capacitances, Single-Stage Amplifiers: Common-Source (with various loads), Common-Gate, and Source Follower stages, Cascode Amplifiers: Telescopic and Folded Cascode; Gain and frequency response analysis.		**12**
	Unit 2: Current Mirrors & Differential Amplifiers Current Mirrors: Basic, Cascode, and Active current mirrors; Mismatch and scaling, Voltage References: Supply-independent biasing; Temperature-independent references (Proportional to Absolute Temperature - PTAT) and Bandgap references, Differential Pairs: Common-mode and Differential-mode analysis, CMRR, and Differential pair with active loads.		**12**
	Unit 3: Op-Amp Design & Stability Two-Stage CMOS Op-Amp: Design procedure, transistor sizing, and power consumption, Feedback & Stability: Review of loop gain; Stability criteria and Phase Margin, Frequency Compensation: Miller compensation, Pole-splitting, and Zero-nulling techniques, Performance Metrics: Slew rate, PSRR (Power Supply Rejection Ratio), Noise, and Output swing.		**12**
	Unit 4: Advanced Building Blocks & Layout Comparators: Static and dynamic characteristics; Two-stage and latch-based comparators, Switched Capacitor Circuits: The MOS switch, charge injection, and clock feedthrough; Switched-capacitor integrators, Data Converters: Introduction to Nyquist-rate, D/A and A/D architectures (Flash, SAR), Analog Layout: Matching techniques (Common-centroid, Interdigitation), Guard rings, and Latch-up prevention.		**12**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Course Code: VL 5102	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	Y	N
Type of Course	Theory		
Course Title	**Embedded Systems Design (VL 5102)**		
Course Objectives	• To provide students with fundamental knowledge of embedded systems, processor architectures, memory organization, communication interfaces, and modern digital hardware technologies used in real-time applications. • To develop the ability to design, optimize, verify, and test embedded systems using appropriate hardware/software methodologies, communication protocols.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the fundamentals of embedded systems, processor architectures, memory organization, communication buses.	Knowledge/Comprehension (Level I/Level-II)
CO2	Apply embedded system design methodologies, interfacing techniques, and communication protocols for developing real-time embedded applications.	Analysis (Level-IV)
CO3	Analyse system performance, cache behavior, signal integrity, timing constraints, and fault models in embedded hardware systems.	Application (Level-III)
CO4	Design, optimize, verify, and evaluate embedded systems with respect to area, power, timing, reliability, and testability requirements.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**	**Summer**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	1	0	4	48
Prerequisite course codes with course names	**Digital Electronics (EC 2401), Introduction to Microprocessors (EC 3501)**				

Text Books		
1.	Title	Digital Design: An Embedded Systems Approach Using Verilog
	Author	Peter J. Ashenden
	Publisher	ELSEVIER, Morgan Kaufmann Publication,
	Edition	2008
2.	Title	Computers as Components: Principles of Embedded Computing System Design
	Author	Wayne Wolf
	Publisher	Morgan Kaufmann
	Edition	3rd Edition
Reference Books		
1.	Title	The 8051 Microcontroller and Embedded Systems
	Author	Muhammad Ali Mazidi
	Publisher	Pearson Education
	Edition	2nd Edition

Course Contents	**Unit 1: Fundamentals of Digital & Embedded System Design** Digital Systems and Embedded Systems: Introduction to Embedded Systems, Characteristics of Embedded Systems, Applications of Embedded Systems, Design Methodology and Design Metrics: Embedded System Design Methodology, Design Flow, Design Metrics, Embedded System Specialties. Memory Concepts: Concepts and Types of Memory, Cache Memory. Integrated Circuit Technologies: Logic Families, ASICs, PLDs, PALs, CPLDs, FPGA. Packaging: Packaging and Circuit Boards, Interconnection and Signal Integrity, Differential Signalling.	**12**
	Unit 2: Embedded Processors and Computer Organization General Purpose and Embedded Processors: General Purpose Processor, System on Chip (SoC), Embedded Computer Organization, ARM Architecture: ARM9 Architecture, ARM Microcontrollers and Processor Cores. Instruction Handling and Memory Interfacing: Instructions and Data Handling: Interfacing with Memory. Interrupts and Timing: Interrupts, Timers, ARM Bus Architecture.	**12**
	Unit 3: I/O Systems and Communication Protocols I/O Devices and Controllers: I/O Devices, Controllers, Simple I/O Controllers, Autonomous I/O Controllers. Bus Structures: Parallel Buses, Multiplexed Buses, Tristate Buses, Open-Drain Buses, Bus Protocols. Serial and Wireless Communication: Serial Transmission Techniques, Serial Communication Standards, Wireless Protocols. Advanced Communication Buses: CAN Bus, Advanced Buses	**12**
	Unit 4: Embedded System Design Flow, Optimization and Testing Design Methodology and Flow: Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification. Implementation and Physical Design: Synthesis, Physical Design. Design Optimization: Area Optimization, Timing Optimization, Power Optimization. Design for Testability: Design for Test (DFT), Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST). Nontechnical Issues: Cost, Reliability, Safety and Standards, Ethical and Commercial Issues.	**12**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5103	Open Elective Course: (Y/N)	Departmental Core Course: (Y/N)	Departmental Elective Course: (Y/N)
	N	Y	N
Type of Course	Theory Course		
Course Title & Code	**Semiconductor Device Modelling** (VL5103)		
Course Objectives	• To introduce students to the physics of semiconductors. • To provide students the insight useful for understanding new semiconductor devices and technologies.		

Course Outcomes		Cognitive Levels
CO1	To analyze MOS and its operation on the basis of physical operation	Knowledge/Comprehension (Level I/Level-II)
CO2	To develop a physics-based knowledge on the basic fundamentals in the course	Application (Level-III)
CO3	To relate a 2nd order effect or deviation from ideal behavior in circuit level to device physics concept learnt in the course	Analysis (Level-IV)
CO4	To understand, articulate and demonstrate new ideas given in research literature of the field	Synthesis/Evaluation (Level-VI/Level-V)

Semester	I	Summer			
Contact Hours	Lecture	Tutorial	Practical	Credits	Total Teaching Hours
	3	1	0	4	48
Prerequisite course codes with course names	Introduction to Semiconductor Devices(EC 2403)				

Text Books		
1.	Title	Operation and Modeling of the MOS Transistor
	Author	Yannis Tsividis
	Publisher	Oxford University Press
	Edition	3rd Edition
2.	Title	MOSFET models for VLSI Circuit Simulation
	Author	N. Arora
	Publisher	Springer-Verlag
	Edition	1st Edition

Reference Books		
1.	Title	Introduction to Semiconductor Device Modeling
	Author	C. Snowden
	Publisher	World Scientific
	Edition	1986

	UNIT I: Two Terminal MOS Structure	12

Course Contents	Contact Potential: Overview, flat-band voltage, potential and charge balance, channel charge, accumulation, depletion, inversion, threshold voltage, small signal capacitances.	
	UNIT II: Three Terminal MOS Structure Effect of channel-body potential, body effect, inversion regions, contacting the inversion layer, region of inversion: approximate limits, threshold voltage, V_{CB} control point of view, pinch-off voltage.	12
	UNIT III: Four Terminal MOS Transistor Complete charge-sheet model, simplified charge-sheet model, strong and weak inversion approximation to the channel current, effective surface mobility, field dependence of the surface mobility, breakdown.	12
	UNIT IV: Small Dimensional Effects Long- and short-channel MOS transistor, carrier velocity saturation, channel length modulation, charge sharing, DIBL, threshold voltage rolls-off, narrow channel effects, punch through, hot-carrier effects, GIDL, scaling: constant field and constant voltage scaling, non-scaling effects, modern scaling.	12
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Type of Course	Theory				
Course Title	**VLSI System Design (VL 5104)**				
Course Objectives	• This course provides a comprehensive study of the design of very-large-scale integrated (VLSI) systems. It covers the entire design flow, from system-level specification and architectural design using HDLs (Verilog/System Verilog) to circuit-level implementation and physical layout. • Key focus areas include timing analysis, power optimization, and the use of industry-standard Electronic Design Automation (EDA) tools.				
Course Outcomes					**Cognitive Levels**
CO1	**Model** complex digital systems using Verilog HDL and perform functional verification.				Knowledge/Comprehension (Level I/Level-II)
CO2	**Analyze** the performance of CMOS logic circuits in terms of area, speed, and power.				Analysis (Level-IV)
CO3	**Implement** the back-end design flow including floor planning, placement, and routing using EDA tools.				Application (Level-III)
CO4	**Evaluate** the testability of an integrated circuit and incorporate DFT features into the design.				Synthesis/Evaluation (Level-VI/Level-V)
Semester	**I**		**Summer**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course	Signals and Systems (EC2301), Digital Signal Processing (EC2404)				

<table>
<tr><td colspan="2">names</td><td colspan="2"></td></tr>
<tr><td colspan="4">Text Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="2">CMOS VLSI Design: A Circuits and Systems Perspective</td></tr>
<tr><td>Author</td><td colspan="2">N.H.E. Weste and D.M. Harris</td></tr>
<tr><td>Publisher</td><td colspan="2">Pearson</td></tr>
<tr><td>Edition</td><td colspan="2">4th edition</td></tr>
<tr><td rowspan="4">2.</td><td>Title</td><td colspan="2">Digital Integrated Circuits: A Design Perspective</td></tr>
<tr><td>Author</td><td colspan="2">Jan M. Rabaey, A. Chandrakasan, and B. Nikolic</td></tr>
<tr><td>Publisher</td><td colspan="2">Pearson</td></tr>
<tr><td>Edition</td><td colspan="2">2nd ed.</td></tr>
<tr><td colspan="4">Reference Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="2">Modern VLSI Design: IP-Based Design,</td></tr>
<tr><td>Author</td><td colspan="2">Wayne Wolf</td></tr>
<tr><td>Publisher</td><td colspan="2">Prentice Hall.</td></tr>
<tr><td>Edition</td><td colspan="2">4th edn.</td></tr>
<tr><td rowspan="3">Course Contents</td><td colspan="2">Unit 1: CMOS Logic and Manufacturing
CMOS Inverter: Static and dynamic characteristics; Switching threshold, noise margins, and delay estimation, Combinational & Sequential Logic: Static CMOS, Ratioed logic, Pass-transistor logic, and Dynamic CMOS circuits, CMOS Fabrication: Overview of the fabrication process (N-Well, P-Well, Twin-tub); Design rules and Stick diagrams, Interconnects: Modeling of resistive and capacitive parasitics; Interconnect delay and scaling issues.</td><td>9</td></tr>
<tr><td colspan="2">Unit 2: HDL Modeling and Digital System Design
Verilog/System Verilog: Behavioural, Dataflow, and Structural modeling; Writing synthesizable code and test benches, Data Path Subsystems: Design of high-speed adders (Carry Look-ahead, Wallace Tree), multipliers, and shifters, Memory Structures: SRAM, DRAM, and ROM architecture; Sense amplifiers and decoders, Control Unit Design: Finite State Machines (FSMs) and Mealy/Moore architectures.</td><td>9</td></tr>
<tr><td colspan="2">Unit 3: Physical Design Automation
Design Flow: The VLSI Design Cycle (Synthesis → Floor planning → Placement → Routing), Partitioning and Floor planning: Algorithms for chip partitioning; Slicing and non-slicing floors; Pin assignment, Placement and Routing: Global and detailed routing; Clock Tree Synthesis (CTS) for skew minimization, Physical Verification: Design Rule Check (DRC), Layout vs. Schematic (LVS), and parasitic extraction (PEX).</td><td>9</td></tr>
</table>

	Unit 4: Timing, Power, and Testability Timing Analysis: Setup and hold time constraints; Static Timing Analysis (STA), Low Power Design: Sources of power dissipation; Voltage scaling, clock gating, and power-down modes, Design for Testability (DFT): Fault models (stuck-at faults); Scan chains, Built-In Self-Test (BIST), and Boundary Scan (JTAG), System-on-Chip (SoC): Introduction to IP cores, bus protocols (AMBA), and hardware-software co-design.	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5201	Open Elective Course: (Y/N)	Departmental Core Course: (Y/N)	Departmental Elective Course: (Y/N)		
	N	Y	N		
Type of Course	Theory Course				
Course Title & Code	**Digital CMOS IC Design** (VL 5201)				
Course Objectives	● To get Fundamental idea of analog circuits, like, basic amplifiers, current mirrors, differential amplifiers etc. ● To learn static and switching characteristics of the CMOS Inverter, ● To learn about the optical sources. ● To assimilate the operation of pass transistor logic and transmission gates, different types of Memory and its decoder Circuits.				
Course Outcomes					Cognitive Levels
CO1	To understand the operation and characteristics of CMOS devices and fundamental digital CMOS logic circuits.				Knowledge/Comprehension (Level I/Level-II)
CO2	To design and evaluate combinational and sequential CMOS circuit considering power, delay and area constraints.				Analysis (Level-IV)
CO3	To apply VLSI design methodologies and CAD tools for schematic design, simulation and layout of digital CMOS integrated circuits.				Application (Level-III)
CO4	To investigate advanced CMOS design issues such as scaling effects, low-power techniques, reliability challenges in modern IC technologies.				Synthesis/Evaluation (Level-VI/Level-V)
Semester	II		Winter		
Contact Hours	Lecture	Tutorial	Practical	Credits	Total Teaching Hours
	3	1	0	4	48
Prerequisite course codes with course names	Digital Electronics (EC 2401)				
Text Books					
1.	Title	CMOS Digital Integrated Circuits: Analysis and Design			
	Author	Sung-Mo Kang , Yusuf Leblebici			

	Publisher	McGraw-Hill Higher Education; 41st edition (1 December 2002)	
	Edition	2002	
2.	Title	Digital system design- A design perspective	
	Author	Rabaey, Chandrakasan and Milokic	
	Publisher	Pearson education, India.	
	Edition		
Reference Books			
1.	Title	Principles of CMOS VLSI Design, A System Perspective,	
	Author	Neil H.E.Weste and Kamran Eshraghian	
	Publisher	Pearson Education, India	
	Edition		
2.	Title	CMOS Circuit Design, Layout and simulation	
	Author	J. Baker, D.E. Boyce.,	
	Publisher	wiely	
	Edition	2009	
Course Contents	**UNIT I:** Introduction to MOSFETs technology: Process flow and masking steps for MOS, Electrical behaviour of MOS transistors and CMOS fabrication technologies (well process, SOI and scaling), Latch up in CMOS technology. CMOS Inverter: Design, analysis of NMOS inverter (resistive, enhancement and depletion load, CMOS inverters; transfer characteristics, Noise margins, , rationing of transistor size, logic voltage levels, rise and fall of delays, Propagation Delay, Power Consumption.		12
	UNIT II: Layout and stick diagram: Layout Design Rules: Lambda and micron-based design rules- stick diagram, Layer properties of various conducting layers in MOS and CMOS technology (diffusion, poly-silicon and metal), Layout design of different CMOS circuit, area estimation. Design styles, design issues. Combinational Circuits: Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (NAND, NOR gates), complex gates, Pass Transistor logic, Transmission gate, Dynamic MOS design: pseudo NMOS logic, (Half and Full adder), Multiplexer, XOR, XNOR.		12
	UNIT III: Sequential MOS Logic and Memory Design: Static latches; Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. clocked CMOS (C2 MOS) logic, domino logic, NORA, TSPC, advance dynamic logic circuits.		12
	UNIT IV: Clock distribution and clock schemes in VLSI chips, Memory Design: ROM & RAM cells. Energy recovery and adiabatic logic circuits Logical Effort: Logical Effort of Different Digital Circuit Design, Input capacitance, Logical and Electrical effort, parasitic delay, Single stage and Multistage with and without branch network. Design of minimum delay and optimization of best stages.		12

Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5202	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	Y	N
Type of Course	Theory		
Course Title	**Semiconductor IC Technology (VL 5202)**		
Course Objectives	• To provide knowledge about semiconductor materials, crystal growth, and wafer preparation techniques used in IC fabrication. • To understand semiconductor fabrication processes such as oxidation, diffusion, epitaxy, lithography, etching, and ion implantation. • To study metallization, thin film deposition, and process integration techniques for semiconductor devices. • To familiarize students with fabrication technologies of MOSFET, Bipolar, MESFET, MEMS devices and challenges in modern IC manufacturing.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the physics of semiconductor materials, crystal growth, wafer preparation, and clean room technology used in semiconductor device fabrication.	Knowledge/Comprehension (Level-I/Level-II)
CO2	Analyze semiconductor fabrication processes including epitaxy, oxidation, diffusion, lithography, etching, and ion implantation.	Analysis (Level-IV)
CO3	Apply process integration concepts in fabrication of passive components, Bipolar, MOSFET, MESFET, and MEMS technologies.	Application (Level-III)
CO4	Evaluate IC manufacturing processes including testing, packaging, yield improvement, and future challenges in system-on-chip technologies.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**	**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	1	0	4	48
Prerequisite course codes with course names	Engineering Physics-I (PH 1101)				

Text Books		
1.	Title	Fundamentals of Semiconductor Fabrication
	Author	G. S. May and S. M. Sze
	Publisher	Wiley India
	Edition	2004
2.	Title	Silicon VLSI Technology: Fundamentals, Practice and Modeling
	Author	J. D. Plummer, M. D. Deal and P. B. Griffin
	Publisher	Pearson
	Edition	2000

3.	Title	VLSI Technology	
	Author	S. M. Sze	
	Publisher	TMH	
	Edition	2nd	
4.	Title	Semiconductor Devices: Physics and Technology	
	Author	S. M. Sze	
	Publisher	Wiley India	
	Edition	2nd	
Reference Books			
1.	Title	Semiconductor Integrated Circuit Processing Technology	
	Author	W. R. Runyan and K. E. Bean	
	Publisher	Addison Wesley	
	Edition	1990	
2.	Title	The Science and Engineering of Microelectronic Fabrication	
	Author	S. A. Campbell	
	Publisher	Oxford University Press	
	Edition	1996	
3.	Title	Fundamentals of Microfabrication	
	Author	M. J. Madou	
	Publisher	CRC Press	
	Edition	2nd	
Course Contents	**UNIT I: Semiconductor Materials, Crystal Growth and Wafer Preparation** Historical perspective and overview of semiconductor processing technology; semiconductor materials and basic device fabrication concepts; crystal growth techniques: Czochralski and Float Zone methods; silicon wafer fabrication and wafer specifications; basic properties of silicon wafers; clean room concepts and classifications; contamination control; wafer cleaning techniques and RCA cleaning process.	**12**	
	UNIT II: Semiconductor Fabrication Processes Epitaxy and epitaxial growth techniques; thermal oxidation of silicon and oxidation kinetics; photolithography: optical lithography, masks, photoresists, exposure and development; wet and dry etching techniques; thin film deposition methods: CVD, PVD, sputtering; diffusion process and impurity profile analysis; ion implantation and annealing techniques.	**12**	
	UNIT III: Process Integration and Device Fabrication Technologies Metallization techniques and contact formation; process integration concepts; fabrication of passive components; Bipolar IC technology; MOSFET fabrication technology; CMOS fabrication process; MESFET technology; MEMS fabrication technology and micromachining basics.	**12**	
	UNIT IV: IC Manufacturing, Packaging and Future Trends IC manufacturing flow; electrical testing and reliability analysis; semiconductor packaging technologies; yield and yield enhancement techniques; challenges in deep submicron and nanoscale integration; system-on-chip (SoC) technology; future trends in semiconductor IC fabrication and emerging technologies.	**12**	

Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5203	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Low Power VLSI (VL 5203)**		
Course Objectives	• This course addresses the critical challenge of power dissipation in modern integrated circuits. It explores the physics of power loss—including static leakage and dynamic switching—and provides a systematic approach to power reduction at multiple levels of abstraction: from device and circuit levels up to architectural and system levels. • Students will learn to design energy-efficient systems for mobile devices, IoT, and high-performance computing without compromising the required performance.		

Course Outcomes		**Cognitive Levels**
CO1	Identify and Quantify the different sources of power dissipation in a CMOS digital circuit.	Knowledge/Comprehension (Level I/Level-II)
CO2	Use power estimation tools to analyze the switching activity and peak power of a VLSI system.	Analysis (Level-IV)
CO3	Optimize digital architectures using clock gating and DVFS to meet strict energy budgets.	Application (Level-III)
CO4	Evaluate the trade-offs between area, delay, and power (the PDP and EDP metrics) for various design decisions.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**		**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	1	0	4	48
Prerequisite course codes with course names	Computer Organization and Architecture (EC 3672), Advanced Microprocessor (EC 3671)				

Text Books		
1.	Title	Low-Power CMOS VLSI Circuit Design
	Author	Kaushik Roy and Sharat Prasad,
	Publisher	Wiley
	Edition	2nd Edition
2.	Title	Low Power Digital CMOS Design,
	Author	Anantha Chandrakasan and Robert Brodersen
	Publisher	Kluwer Academic Publishers

<table>
<tr><td></td><td>Edition</td><td colspan="2">2nd Edition</td></tr>
<tr><td colspan="4">Reference Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="2">Practical Low Power Digital VLSI Design</td></tr>
<tr><td>Author</td><td colspan="2">Behzad Razavi</td></tr>
<tr><td>Publisher</td><td colspan="2">Springer</td></tr>
<tr><td>Edition</td><td colspan="2">Second edition</td></tr>
<tr><td rowspan="4">Course Contents</td><td colspan="2">Unit 1: Physics of Power Dissipation

Sources of Power Consumption: Dynamic power (switching and short-circuit), Static power (sub-threshold leakage, gate-oxide tunneling, BTBT), and Glitching power, Impact of Scaling: Constant field vs. constant voltage scaling; The "Power Wall" and its implications on multicore processing, Probabilistic Power Analysis: Modeling signal activity, transition density, and statistical techniques for power estimation.</td><td>12</td></tr>
<tr><td colspan="2">Unit 2: Circuit and Logic Level Optimization

Dynamic Power Reduction: Supply voltage scaling, Multi-voltage domains, and Capacitance minimization, Leakage Control Techniques: Multi-threshold CMOS (MTCMOS), Variable-threshold CMOS (VTCMOS), and Transistor stacking (The Stack Effect) Logic Style Comparison: Static CMOS vs. Pass-transistor logic and Dynamic logic in the context of power efficiency, Glitch Reduction: Path balancing and logic restructuring to eliminate spurious transitions.</td><td>12</td></tr>
<tr><td colspan="2">Unit 3: Architectural and System Level Power Management

Dynamic Voltage and Frequency Scaling (DVFS): Principles, algorithms, and hardware overhead, Clock Gating and Power Gating: Implementation of sleep modes, state retention cells, and isolation cells, Memory Power Management: Low-power SRAM designs, banked architectures, and data retention in caches, Bus Encoding: Techniques like Bus-Invert coding to reduce switching activity on high-capacitance I/O lines.</td><td>12</td></tr>
<tr><td colspan="2">Unit 4: Advanced Topics and EDA Tools

Adiabatic Switching: Principles of energy recovery and charge recycling, Software Power Estimation: Instruction-level power analysis and energy-efficient software design, Standard Power Formats: Introduction to UPF (Unified Power Format) and CPF (Common Power Format) for EDA tool flows, Future Trends: Energy harvesting, sub-threshold computing for ultra-low-power sensors, and FinFET/GAAFET impacts on power.</td><td>12</td></tr>
<tr><td>Course Assessment</td><td>Total Marks=100</td><td colspan="2">Continuous Evaluation 20%
Mid Semester 30%
End Semester 50%</td></tr>
</table>

Course Code: VL 5204	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	Y	N
Type of Course	Theory Course		
Course Title & Code	Real Time Operating System (VL 5204)		
Course Objectives	• To understand the basics of real-time operating systems and need of real time operating systems (RTOS). • To design and develop simple embedded applications using RTOS environments.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the basics of real time operating systems	Knowledge/Comprehension (Level I/Level-II)
CO2	Familiarize task management strategies and real-time scheduling algorithms.	Analysis (Level-IV)
CO3	Learn the programming logic of modelling Process based on range of OS features	Knowledge/Comprehension (Level I/Level-II)
CO4	Develop real time applications using RTOS	Application (Level-III)

Semester	**II**	**Winter**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	**Embedded system** (EC 4774)				

Text Books		
1.	Title	Embedded Real Time Systems: Concepts, Design & Programming
	Author	Dr.K.V.K.K. Prasad,
	Publisher	Dreamtech Publication
	Edition	2007
2.	Title	Modern Operating Systems
	Author	Andrew S. Tanenbaum
	Publisher	Prentice Hall Publication
	Edition	2001
Reference Books		
1.	Title	Embedded Systems Architecture, Programming and design

	Author	Raj Kamal	
	Publisher	Tata Mcgraw-Hill Publication	
	Edition	1999	
Course Contents	**UNIT I:** Introduction to operating systems (OS), Functions of OS, General purpose operating systems functionalities, system calls, architecture, OS for single processor and multiprocessor systems		9
	UNIT II: Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Software Development Process Life Cycle and its Model		9
	UNIT III: Real-Time Software Concepts, Kernel Structure, Tasks, task states and transitions, task attributes, types, task control block, task creation, deletion, and task priorities. Introduction to real-time scheduling		9
	UNIT IV: Discussions on Basics of Linux supportive RTOS – uCOS-C Executive for development of RTOS Application – Case study		9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Course Code: VL 5151	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Digital System Design (VL 5151)**		
Course Objectives	• To introduce the principles of sequential logic design and finite state machine modeling. • To understand synchronous sequential circuit analysis, state machine synthesis, and clock skew concepts. • To provide knowledge of programmable logic devices such as PLDs, CPLDs, and FPGAs. • To develop hardware design skills using VHDL and logic simulation tools.		

Course Outcomes		**Cognitive Levels**
CO1	Design and analyze Mealy and Moore finite state machines using state diagrams and flip-flop based implementations.	Application/Analysis (Level-III/Level-IV)
CO2	Analyze synchronous sequential circuits, metastability effects, and clock skew issues in digital systems.	Analysis (Level-IV)
CO3	Understand the architecture and applications of PLDs, CPLDs, and FPGA-based digital system implementation.	Knowledge/Comprehension (Level-I/Level-II)
CO4	Develop RTL level combinational and sequential digital circuits using VHDL and logic simulation tools.	Synthesis/Application (Level-V/Level-III)

<table>
<tr><td colspan="2">Semester</td><td colspan="2">I</td><td colspan="3">Summer</td></tr>
<tr><td colspan="2" rowspan="2">Contact Hours</td><td>Lecture</td><td>Tutorial</td><td>Practical</td><td>Credits</td><td>Total Teaching Hours</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>3</td><td>36</td></tr>
<tr><td colspan="2">Prerequisite course codes with course names</td><td colspan="5">Digital Electronics
Switching Theory and Logic Design
VLSI Design Fundamentals</td></tr>
<tr><td colspan="7">Text Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="5">Digital Design: Principles and Practices</td></tr>
<tr><td>Author</td><td colspan="5">J. F. Wakerly</td></tr>
<tr><td>Publisher</td><td colspan="5">Pearson</td></tr>
<tr><td>Edition</td><td colspan="5">4th Edition, 2008</td></tr>
<tr><td rowspan="4">2.</td><td>Title</td><td colspan="5">FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version</td></tr>
<tr><td>Author</td><td colspan="5">Pong P. Chu</td></tr>
<tr><td>Publisher</td><td colspan="5">Wiley-Interscience</td></tr>
<tr><td>Edition</td><td colspan="5">1st Edition, 2008</td></tr>
<tr><td colspan="7">Reference Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="5">Fundamentals of Digital Logic with VHDL Design</td></tr>
<tr><td>Author</td><td colspan="5">Stephen Brown and Zvonko Vranesic</td></tr>
<tr><td>Publisher</td><td colspan="5">McGraw Hill</td></tr>
<tr><td>Edition</td><td colspan="5">3rd Edition</td></tr>
<tr><td rowspan="4">2.</td><td>Title</td><td colspan="5">Digital Systems Design Using VHDL</td></tr>
<tr><td>Author</td><td colspan="5">Charles H. Roth Jr.</td></tr>
<tr><td>Publisher</td><td colspan="5">Cengage Learning</td></tr>
<tr><td>Edition</td><td colspan="5">2nd Edition</td></tr>
<tr><td rowspan="4">3.</td><td>Title</td><td colspan="5">FPGA-based System Design</td></tr>
<tr><td>Author</td><td colspan="5">Wayne Wolf</td></tr>
<tr><td>Publisher</td><td colspan="5">Pearson</td></tr>
<tr><td>Edition</td><td colspan="5">2004</td></tr>
<tr><td rowspan="4">Course Contents</td><td colspan="5">UNIT I: Principles of Sequential Logic Design and FSM Concepts
Introduction to sequential logic circuits; latches and flip-flops; concept of finite state machines (FSM); Moore and Mealy state machine models; state machine structures; state diagrams and state tables; analysis of state machines using D and J-K flip-flops; state minimization and state assignment techniques.</td><td>9</td></tr>
<tr><td colspan="5">UNIT II: Synchronous Sequential Circuit Design and Clock Issues
Clocked synchronous state machine design; FSM synthesis using transition lists; metastability in sequential circuits; synchronization techniques; setup time and hold time constraints; clock skew and its effects on synchronous digital systems; timing analysis and design considerations for reliable operation.</td><td>9</td></tr>
<tr><td colspan="5">UNIT III: Programmable Logic Devices and FPGA Architectures
Overview of programmable logic devices (PLDs); architecture and characteristics of CPLDs and FPGAs; FPGA logic blocks, routing architecture, and programmable interconnects; FPGA design flow; comparison of PLDs, CPLDs, and FPGAs; applications of programmable logic devices in digital system design.</td><td>9</td></tr>
<tr><td colspan="5">UNIT IV: RTL Design and VHDL-Based Digital System Design</td><td>9</td></tr>
</table>

	RTL level combinational circuit design; regular sequential circuit design; introduction to VHDL; behavioral, dataflow, and structural modeling styles; design examples using VHDL; simulation and verification using logic simulation tools; synthesis concepts and FPGA implementation flow.	
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5152	Open Elective Course: (Y/N)	Departmental Core Course: (Y/N)	Departmental Elective Course: (Y/N)
	N	N	Y
Type of Course	Theory Course		
Course Title & Code	**Signal Processing for Embedded Systems** (VL 5152)		
Course Objectives	• To illustrate various signal processing algorithms and transforms • To integrate transforming techniques like folding/ unfolding, retiming, parallel processing to achieve faster computations and better efficiency • To judge the performance of the algorithms using various DSP processor architectures		

Course Outcomes		Cognitive Levels
CO1	To understand the fundamental DSP techniques such as filtering, FFT, DCT, and wavelet transforms for embedded signal processing applications.	Knowledge/Comprehension (Level I/Level-II)
CO2	To design design efficient DSP architectures using pipelining, parallel processing, retiming, folding, and unfolding techniques.	Analysis (Level-IV)
CO3	To develop real-time DSP applications using embedded DSP processors and hardware interfacing techniques.	Application (Level-III)
CO4	To implement DSP-based applications including adaptive filtering, noise cancellation, FFT, and communication signal processing.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	I	Summer			
Contact Hours	Lecture	Tutorial	Practical	Credits	Total Teaching Hours
	3	0	0	3	36
Prerequisite course codes with course names	Embedded Systems (EC 4774); Digital Signal Processing (EC3503)				

Text Books		
1.	Title	Digital Signal Processors, architectures, implementations, and applications
	Author	Sen M. Kuo and Woon-Seng Gan
	Publisher	Prentice-Hall
	Edition	1999
2.	Title	The Digital Signal Processing Handbook
	Author	V. Madisetti

	Publisher	IEEE press	
	Edition	2000	
Reference Books			
1.	Title	Theory and application of Digital signal Processing	
	Author	Lawrence R. Rabiner and Bernard Gold	
	Publisher	Prentice-Hall of India	
	Edition	2006	
Course Contents	UNIT I: Digital Signal Processing Overview, Convolution, Correlation, Digital filters, DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph, iteration bounds.		9
	UNIT II: Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming, Folding, Unfolding, Algorithmic strength reduction in Filters and Transforms, Parallel FIR filters, Fast FIR algorithms, Discrete cosine transform and Inverse DCT, Parallel processing for IIR filters, Pipelined adaptive digital filters.		9
	UNIT III: Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, real time implementation considerations, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management.		9
	UNIT IV: On chip resources, programming considerations, Real time implementations, Applications of DSP systems: FIR filters, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.		9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Course Code: VL 5153	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Microcontroller for Embedded Systems (VL 5153)**		
Course Objectives	• To provide knowledge of ARM processor architecture, instruction sets, memory management, and embedded programming concepts. • To develop the ability to design and optimize embedded software using ARM assembly language, cache management, and memory management techniques.		

Course Outcomes		**Cognitive Levels**
CO1	Understand ARM architecture, processor organization, registers, interrupts, and instruction pipeline.	Knowledge/Comprehension (Level I/Level-II)
CO2	Apply ARM and Thumb instruction sets for embedded software development and interfacing applications	Analysis (Level-IV)
CO3	Analyse ARM assembly programs, instruction scheduling, register allocation, cache behaviour, and memory management operations.	Application (Level-III)
CO4	Design and optimize embedded applications using ARM processors with efficient memory management and context switching techniques	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**	**Summer**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	0	36
Prerequisite course codes with course names	Digital Electronics (EC 2401), Introduction to Microprocessors (EC 3501)				

Text Books		
1.	Title	ARM System-on-Chip Architecture
	Author	Steve Furber
	Publisher	Pearson Education
	Edition	2nd Edition
2.	Title	ARM Architecture Reference Manual
	Author	David Seal
	Publisher	Addison-Wesley
	Edition	Latest Edition

Reference Books		
1.	Title	Embedded Systems Design with ARM Cortex-M Microcontrollers
	Author	Yifeng Zhu
	Publisher	Pearson
	Edition	Latest Edition

Course Contents		
	UNIT I: ARM Architecture and Organization ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.	**9**
	UNIT II: ARM and Thumb Instruction Set Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. Thumb	**9**

	Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions	
	UNIT III: ARM Programming Techniques Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating-Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.	**9**
	UNIT IV: Memory Management and Cache Cache Architecture, Policies, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5154	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Embedded Networking (VL 5154)**		
Course Objectives	• To provide knowledge of embedded communication protocols, network interfaces, wired and wireless networking techniques used in embedded systems. • To develop the ability to design and implement embedded networking applications using serial buses, Ethernet, Internet protocols, CAN, USB, and wireless sensor networks.		

Course Outcomes		**Cognitive Levels**
CO1	Understand embedded communication protocols, serial interfaces, USB, CAN, Ethernet, and wireless sensor network fundamentals	Knowledge/Comprehension (Level I/Level-II)
CO2	Apply networking protocols and embedded interfaces for communication between embedded devices and computer networks.	Analysis (Level-IV)
CO3	Analyse network communication, protocol performance, routing methods, timing, and security issues in embedded networking systems.	Application (Level-III)
CO4	Design embedded networking applications using Ethernet, Internet protocols, CAN bus, USB, and wireless sensor network architectures.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**	**Summer**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course	Digital Electronics (EC 2401), Introduction to Microprocessors (EC 3501), Computer Networks (EC 4702)				

names			
Text Books			
1.	Title	Embedded Systems: Architecture, Programming and Design	
	Author	Raj Kamal	
	Publisher	McGraw Hill Education	
	Edition	3rd Edition	
2.	Title	TCP/IP Lean: Web Servers for Embedded Systems.	
	Author	Jeremy Bentham	
	Publisher	CMP Books	
	Edition	2nd Edition	
Reference Books			
1.	Title	Computer Networks	
	Author	Andrew S. Tanenbaum	
	Publisher	Pearson Education	
	Edition	5th Edition	
Course Contents	UNIT I: Embedded Communication Protocols: Embedded Networking: Introduction, Serial/Parallel Communication, Serial Communication Protocols RS232 Standard, RS485, Synchronous Serial Protocols, Serial Peripheral Interface (SPI), Inter Integrated Circuits (I2C), PC Parallel Port Programming, ISA/PCI Bus Protocols, Firewire.		**9**
	UNIT II: USB and CAN Bus: USB Bus: Introduction, Speed Identification on the Bus, USB States, USB Bus Communication: Packets, Data Flow Types, Enumeration, Descriptors, PIC18 Microcontroller USB Interface, C Programs. CAN Bus: Introduction, Frames, Bit Stuffing, Types of Errors, Nominal Bit Timing, PIC Microcontroller CAN Interface, Simple Applications with CAN.		**9**
	UNIT III: Ethernet and Internet: Communication Elements of a Network, Inside Ethernet, Building a Network: Hardware Options, Cables, Connections and Network Speed, Design Choices: Selecting Components, Ethernet Controllers, Using the Internet in Local and Internet Communications, Inside the Internet Protocol, Exchanging Messages using UDP and TCP, Serving Web Pages with Dynamic Data, Serving Web Pages that Respond to User Input, Email for Embedded Systems, Using FTP, Keeping Devices and Networks Secure.		**9**
	UNIT IV: Wireless Sensor Networks: Wireless Sensor Networks: Introduction, Applications, Network Topology, Localization, Time Synchronization, Energy Efficient MAC Protocols, SMAC, Energy Efficient and Robust Routing, Data Centric Routing.		**9**
Course	Total Marks=100	Continuous Evaluation 20%	

Assessment		Mid Semester 30% End Semester 50%

Course Code: VL 5155		**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**		**Departmental Elective Course: (Y/N)**
		N	N		Y
Type of Course		Theory Course			
Course Title & Code		FPGA Design (VL 5155)			
Course Objectives		● Understand FPGA architecture and design and implementation styles. ● To get familiarize with different types of FPGA architecture			
Course Outcomes					**Cognitive Levels**
CO1	Understand design and implementation styles				Knowledge/Comprehension (Level I/Level-II)
CO2	Use computer-aided design tools to synthesize, map, place, routing, and download the digital designs on the FPGA board				Application (Level-III)
CO3	Identify and distinguish different special purpose processor architecture				Analysis (Level-IV)
CO4	Understand design of parametrized library cells				Synthesis/Evaluation (Level-VI/Level-V)
Semester		**VIII**		**Summer/Winter**	
Contact Hours		**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
		3	0	0	3	36
Prerequisite course codes with course names		Digital Electronics (EC 2401)			
Text Books					
1.	Title	Field Programmable Gate Arrays			
	Author	John V.Old Field, Richrad C. Dorf,			
	Publisher	John Wiley			
	Edition	1995			
2.	Title	Application Specific Integrated Circuits			
	Author	Michel John Sebastian Smith			
	Publisher	Pearson			
	Edition	1997			
Course Contents	**UNIT I:** Overview of FPGA architectures and technologies, Design styles, Implementation styles, Design Examples using programmable logic devices				9
	UNIT II: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation				9

	UNIT III: Design of Universal block. Design of memory, Floating point multiplier, Barrel shifter, Xilinx Vertex and Spartan - II; Altera FLEX 10k architectures	9
	UNIT IV: Design of parameterized library cells, Implementation and Testing- Xilinx, Actel and Altera FPGA based systems. Design - Case study.	9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5156	Open Elective Course: (Y/N)	Departmental Core Course: (Y/N)	Departmental Elective Course: (Y/N)
	N	N	Y
Type of Course	Theory Course		
Course Title & Code	**VLSI DSP** (VL 5156)		
Course Objectives	• To Understand the overview of DSP concepts. • To Perform Pipelining and parallel processing in FIR systems to achieve high speed and low power. • To Learn and understand the different techniques of power reduction and power estimation.		

Course Outcomes		Cognitive Levels
CO1	To understand and model DSP algorithms using data flow graphs, iteration bound computation, pipelining, parallel processing, retiming, and unfolding techniques for high-speed VLSI implementations.	Knowledge/Comprehension (Level I/Level-II)
CO2	To design optimized VLSI architectures for DSP applications including FIR filters, FFT processors, systolic arrays, and CORDIC-based systems with considerations for throughput, latency, and hardware efficiency.	Analysis (Level-IV)
CO3	To apply folding transformations, register minimization techniques, and bit-level arithmetic architectures such as serial/parallel multipliers and redundant arithmetic for area-efficient DSP hardware realization.	Application (Level-III)
CO4	To evaluate and implement low-power VLSI DSP systems by analyzing power consumption, applying power reduction techniques, and estimating performance-power trade-offs in FPGA/ASIC-based DSP architectures.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	I	Summer			
Contact Hours	Lecture	Tutorial	Practical	Credits	Total Teaching Hours
	3	0	0	3	36

Prerequisite course codes with course names	VLSI Design (EC 3601); Digital Signal Processing (EC3503)		
Text Books			
1.	Title	DSP with FPGA	
	Author	Sung-Mo Kang, Yusuf Leblebici U. Meyer-Baese	
	Publisher	Springer	
	Edition	2004.	
2.	Title	VLSI DSP Systems	
	Author	K. K. Parhi	
	Publisher	Wiley.	
	Edition	2003	
Reference Books			
1.	Title	Understanding Digital Signal Processing	
	Author	R.G. Lyons	
	Publisher	Pearson Education	
	Edition	2004	
Course Contents	UNIT I: Introduction to DSP systems: Representation of DSP algorithms; Iteration Bound: Definition, Examples, Algorithms for computing Iteration bound; Pipelining and Parallel Processing: Definitions, Pipelining and parallel processing of FIR filters, Pipelining and parallel processing for low power		9
	UNIT II: Retiming: Definitions and Properties, Solving system of Inequalities, Retiming techniques; Unfolding: Definition, An algorithm for unfolding, Applications of unfolding; Folding: Definition, Folding transformations, Register minimization techniques, Register minimization in folded architectures;		9
	UNIT III: Systolic Architecture Design: Introduction, Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-Matrix multiplication and 2D systolic array design; CORDIC based Implementations: Architecture, Implementation of FIR filter and FFT algorithm; Bit-Level arithmetic architectures: Parallel multipliers, Bit-serial multipliers		9
	UNIT IV: Bit-Serial FIR filter design and Implementation; Redundant arithmetic: Redundant number representation, Carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures; Low-power design: Theoretical background, Scaling versus power consumption, Power analysis, Power reduction techniques, Power estimation approaches.		9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

<table>
<tr><td rowspan="2">Course Code:
VL 5157</td><td>Open Elective Course: (Y/N)</td><td>Departmental Core Course: (Y/N)</td><td>Departmental Elective Course: (Y/N)</td></tr>
<tr><td>N</td><td>N</td><td>Y</td></tr>
<tr><td>Type of Course</td><td colspan="3">Theory Course</td></tr>
<tr><td>Course Title & Code</td><td colspan="3">Digital IC Design (VL 5157)</td></tr>
<tr><td>Course Objectives</td><td colspan="3">● To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc.,
● To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.
● To learn all important issues related to size, speed and power consumption.</td></tr>
<tr><td colspan="2">Course Outcomes</td><td colspan="2">Cognitive Levels</td></tr>
<tr><td>CO1</td><td colspan="2">To understand the power dissipated in the circuit.</td><td colspan="2">Knowledge/Comprehension (Level I/Level-II)</td></tr>
<tr><td>CO2</td><td colspan="2">To design a circuit to performed a certain functionality with specified speed.</td><td colspan="2">Application (Level-III)</td></tr>
<tr><td>CO3</td><td colspan="2">To identify the critical path of a combinational Circuit</td><td colspan="2">Analysis (Level-IV)</td></tr>
<tr><td>CO4</td><td colspan="2">To convert a combinational block to pipelined circuit and calculate the maximum frequency of the designed circuit.</td><td colspan="2">Synthesis/Evaluation (Level-VI/Level-V)</td></tr>
<tr><td>Semester</td><td colspan="2">I</td><td colspan="2">Summer</td></tr>
<tr><td rowspan="2">Contact Hours</td><td>Lecture</td><td>Tutorial</td><td>Practical</td><td>Credits</td><td>Total Teaching Hours</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>3</td><td>36</td></tr>
<tr><td>Prerequisite course codes with course names</td><td colspan="5">IC Applications(EC 3504)</td></tr>
<tr><td colspan="6">Text Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="4">Digital Integrated Circuit: A design perspective</td></tr>
<tr><td>Author</td><td colspan="4">J. M. Rabaey, A. Chandrakasan, B. Nikolic</td></tr>
<tr><td>Publisher</td><td colspan="4">Pearson Education, Delhi-2005</td></tr>
<tr><td>Edition</td><td colspan="4">2nd Edition</td></tr>
<tr><td rowspan="4">2.</td><td>Title</td><td colspan="4">CMOS VLSI Design</td></tr>
<tr><td>Author</td><td colspan="4">Weste, Neil HE, and David Money Harris</td></tr>
<tr><td>Publisher</td><td colspan="4">Pearson/Addison Wesley, 2010. Geiger</td></tr>
<tr><td>Edition</td><td colspan="4">1st Edition</td></tr>
<tr><td colspan="6">Reference Books</td></tr>
<tr><td rowspan="4">1.</td><td>Title</td><td colspan="4">Low power design methodologies</td></tr>
<tr><td>Author</td><td colspan="4">J. M. Rabaey., and MassoudPedram, eds</td></tr>
<tr><td>Publisher</td><td colspan="4">Springer Science & Business Media, 2012</td></tr>
<tr><td>Edition</td><td colspan="4">1st Edition</td></tr>
</table>

Course Contents	UNIT I: MOS Transistor Principles and CMOS Inverter Introduction, MOS Capacitor Threshold Voltage, MOS (FET) Transistor, Short Channel Transistor, CMOS Inverter Construction, Voltage Transfer Characteristics, Load line Analysis, Noise Margin Analysis, Pass Transistor, Inverter: Transient Response, Dynamic Power, Short Circuit Power, Leakage Power and Transistor Stacks	9
	UNIT II: Combinational Logic Circuits Implementing any Boolean Logic Function, Gate Sizing, Logic Gate Capacitance, Gate Delay, Parasitic Delay, Gate Delay with Load Capacitance, Path Delay Calculation and Optimization, Psuedo NMOS Logic, Domino Logic and Weak Keeper, Transmission Gate Logic, Gate Sizing for Large Circuits.	9
	UNIT III: Arithmetic Building Blocks Ripple Adder Introduction, Full Adder Circuit Implementation, Full Adder Optimization, Carry Select Adder, Two's Complement Arithmetic, Array Multiplier: Timing Analysis, Carry Save Multiplier: Signed Multiplication.	9
	UNIT IV: Sequential Logic Circuits Introduction to Pipelining, Time Borrowing, Master Slave Flip Flop, Flip-Flop Timing Parameters, Alternate Circuit Implementation, Clock Overlap, C2MOS Flip Flop, Flip Flop Characterization, Max and Min Delay of Flip Flop Based Systems, Flip Flop Min Delay Constraints, Latch – Max and Min Delay Constraints, Latch-Timing Analysis with Skew.	9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5158	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**MEMS and Microsystem Technology (VL 5158)**		
Course Objectives	• This course introduces the design, fabrication, and application of Micro-Electro-Mechanical Systems (MEMS). It covers the physical scaling laws governing micro-scale phenomena, the specialized cleanroom fabrication techniques (like bulk and surface micromachining), and the integration of sensors and actuators into functional microsystems. • Students learn how to transition from traditional "macro" engineering to the "micro" domain where surface forces dominate over gravity.		

Course Outcomes		**Cognitive Levels**
CO1	**Select** appropriate micro fabrication processes (bulk vs. surface) based on the structural requirements of a device.	Knowledge/Comprehension (Level I/Level-II)

CO2	**Design** and analyze the performance of common MEMS sensors such as accelerometers and pressure sensors.	Analysis (Level-IV)
CO3	**Critique** different packaging solutions for protecting sensitive MEMS components from the environment.	Application (Level-III)
CO4	**Evaluate** the impact of scaling on various physical parameters when designing micro-scale devices.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**		**Summer**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	Linear algebra and differential equations , Solid State Devices: Basics of semiconductor physics,				

Text Books		
1.	Title	MEMS and Microsystems: Design and Manufacture
	Author	Tai-Ran Hsu
	Publisher	McGraw-Hill
	Edition	2nd Ed
2.	Title	Microsystem Design, Springer.
	Author	Stephen D. Senturia
	Publisher	Springer.
	Edition	2nd ed. 2004.
Reference Books		
1.	Title	Micro and Smart Systems
	Author	G. K. Ananthasuresh et al
	Publisher	Wiley India
	Edition	4th Ed

Course Contents	**Unit 1: Introduction and Scaling Laws** Evolution of MEMS: History, motivation, and current market trends (automotive, consumer electronics, and Bio-MEMS), Scaling Laws in Miniaturization: Scaling in geometry, rigid body dynamics, electrostatics, electromagnetics, and heat transfer, Materials for MEMS: Silicon as a structural material; Silicon compounds (SiO_2, Si_3N_4); Polysilicon; Piezoelectric materials and Shape Memory Alloys (SMAs).	**9**
	Unit 2: Microfabrication Technologies Microelectronic Processes: Photolithography, ion implantation, diffusion, and oxidation; Bulk Micromachining: Wet chemical etching (isotropic and anisotropic); Etch-stop technique Surface Micromachining: Sacrificial layer technology; Stiction and its prevention; Specialized Processes: LIGA (Lithography, Electroplating, and Molding), Deep Reactive Ion Etching (DRIE), and wafer bonding.	**9**

	Unit 3: Microsensors and Actuators Mechanical Sensors: Piezoresistive and capacitive pressure sensors; Micro-accelerometers and Gyroscopes; Thermal Sensors: Micro-calorimeters and thermopiles; Microactuators: Electrostatic actuators (comb-drives); Thermal actuators; Piezoelectric and Magnetic actuators; Optical MEMS: Digital Micromirror Devices (DMD) and optical switches.	**9**
	Unit 4: Microsystem Design and Packaging Modeling and Simulation: Lumped element modeling; Introduction to Finite Element Method (FEM) for MEMS analysis; MEMS Packaging: Challenges in micro-scale packaging; Hermetic sealing; Vacuum packaging; Interface Electronics: Signal conditioning for micro-scale signals; Introduction to System-on-Chip (SoC) integration; Case Studies: Inkjet printer heads, Airbag deployment sensors, and Lab-on-a-chip systems.	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5159	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Biomedical Signal and Systems (VL 5159)**		
Course Objectives	• To provide knowledge of biomedical signals, biomedical signal processing techniques, system modelling, and diagnostic analysis methods. • To develop the ability to analyse biomedical signals using filtering, frequency-domain analysis, adaptive processing, segmentation, and pattern classification techniques.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the characteristics of biomedical signals, biomedical systems, signal acquisition problems, and preprocessing methods.	Knowledge/Comprehension (Level I/Level-II)
CO2	Apply filtering, event detection, spectral analysis, and system modelling techniques to biomedical signals.	Analysis (Level-IV)
CO3	Analyse biomedical signals using adaptive filtering, segmentation, frequency-domain characterization, and statistical methods.	Application (Level-III)
CO4	Design and evaluate biomedical signal classification and diagnostic systems using machine learning and pattern recognition approaches	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**I**	**Summer**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**

	3	0	0	3	36
Prerequisite course codes with course names	Signals and Systems (EC 2302), Digital Signal Processing (EC 3503), Probability and Random Process (MA 2401)				

Text Books			
1.	Title	Biomedical Signal Analysis	
	Author	Rangaraj M. Rangayyan	
	Publisher	Wiley-IEEE Press	
	Edition	2nd Edition	
2.	Title	Biomedical Signal Processing and Signal Modeling	
	Author	Eugene N. Bruce	
	Publisher	Wiley	
	Edition	2nd Edition	
Reference Books			
1.	Title	Biomedical Signals and Systems	
	Author	J. N. Gowda	
	Publisher	McGraw Hill Education	
	Edition	Latest Edition	
Course Contents	UNIT I: Introduction to Biomedical Signals and Filtering Techniques Introduction to Biomedical Signals, Nature of Biomedical Signals, Examples of Biomedical Signals: EMG, ECG, EEG, ERPs, PCG, VMG, VAG. Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Concurrent, Coupled and Correlated Processes, Illustration of Problems with Case Studies. Filtering for Removal of Artifacts, Time-Domain Filters, Frequency-Domain Filters, Optimal Filtering, Wiener Filter, Adaptive Filters for Removal of Interference, Applications in ECG Artifact Removal.		**9**
	UNIT II: Event Detection and Biomedical Signal Analysis Event Detection, Detection of Events and Waves, Correlation Analysis of EEG Channels, Cross-Spectral Techniques, Matched Filter, Detection of P Wave, Homomorphic Filtering, ECG Rhythm Analysis, Identification of Heart Sounds, Wave Shape and Waveform Complexity, Analysis of Event-related Potentials, Morphological Analysis of ECG Waves, Envelope Extraction and Activity Analysis, Applications in Normal and Ectopic ECG Beats, Analysis of Exercise ECG.		**9**
	UNIT III: Frequency-Domain Analysis and System Modelling Frequency-Domain Characterization, Fourier Spectrum, Estimation of Power Spectral Density Function, Measures Derived from PSDs. Modeling Biomedical Systems, Point Processes, Parametric System Modeling, Autoregressive and All-Pole Modeling, Pole-Zero Modeling, Electromechanical Models of Signal Generation, Applications in Heart Rate		**9**

	Variability, Spectral Modeling and Analysis of PCG.	
	UNIT IV: Non-Stationary Signal Analysis and Pattern Classification Analysis of Non-Stationary Signals, Time-Variant Systems, Fixed Segmentation, Adaptive Segmentation, Use of Adaptive Filters for Segmentation, Applications in Adaptive Segmentation of EEG and PCG Signals. Pattern Classification and Diagnostic Decision, Supervised and Unsupervised Pattern Classification, Probabilistic Models and Statistical Decision, Logistic Regression Analysis, Training and Test Steps, Neural Networks, Measures of Diagnostic Accuracy and Cost, Reliability of Classifier and Decisions.	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5251	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
		N	Y

Type of Course	Theory Course
Course Title & Code	ASIC Design and Modeling (EC VL5251)
Course Objectives	● To understand the various types of ASICs and ASIC design flow. ● To design programmable ASICs& SOC using EDA tools.

Course Outcomes		**Cognitive Levels**
CO1	Understand different types of ASICs	Knowledge/Comprehension (Level I/Level-II)
CO2	Understand ASIC design flow	Application (Level-III)
CO3	Understand the algorithm for partitioning, floor plan, placement and Routing	Analysis (Level-IV)
CO4	Design programmable ASICs& SOC using EDA tools	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**	**Winter**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36

Prerequisite course codes with course names	Digital Electronics (EC 2401)& VLSI Design (EC 3601)

Text Books

1.	Title	Application Specific Integrated Circuits
	Author	M.J.S.Smith
	Publisher	Pearson

	Edition	200	
2.	Title	Advanced FPGA Design	
	Author	Steve Kilts	
	Publisher	Wiley Inter-Science	
	Edition	2006	
Reference Books			
1.	Title	FPGA-Based Implementation of Signal Processing Systems	
	Author	Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod	
	Publisher	Wiley	
	Edition	2008	
Course Contents	**UNIT I:** Introduction to ASICs, Types of ASICs, ASIC Design Flow, CMOS Logic, FPGA design Flow, Difference between ASIC ad FPGA, RTL coding and synthesis, Logic Modeling		9
	UNIT II: CMOS devices, CMOS design rules, parasitic capacitance, and resistance, Delay Modeling, sizing combinational gates, SPICE Modeling		9
	UNIT III: Logic synthesis, Static Timing Analysis (STA), Design Verification, ASIC floor planning- I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Design Rule Checking (DRC)&Layout Versus Schematic (LVS)		9
	UNIT IV: IP (Intellectual Property)-based Design Flow, FPGA to ASIC conversions, Modeling dynamic/static power, Fault Modeling, Automatic Test Pattern Generation (ATPG), and BIST (Built -In Self-Test)		9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Embedded Computing VL5252

Course Code: VL 5253	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory Course		
Course Title & Code	VLSI EDA Tools (VL 5253)		
Course Objectives	• Understand CMOS VLSI technology. • Develop proficiency in analog and digital circuit design using VLSI EDA tool.		

Course Outcomes	**Cognitive Levels**
CO1 Organize the various equipment and components required for VLSI product development	Knowledge/Comprehension (Level I/Level-II)
CO2 Survey on the libraries available in the CAD tools	Application (Level-III)
CO3 Identify Algorithms for circuit simulation	Analysis (Level-IV)
CO4 Understand the concepts of high-level synthesis	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**		**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	VLSI Design (EC 3601)				

Text Books			
1.	Title	Application Specific Integrated Circuits	
	Author	Michael Smith	
	Publisher	Pearson Education Asia	
	Edition	2000	
Course Contents	**UNIT I:** ASIC design flow, various design entries, IP cores, cross compilers, cell design, stick diagrams, synthesis, place and route, floor planning, power estimation, static timing analysis, dynamic timing analysis		9
	UNIT II: antenna rules, design rule check, electric rule check, schematic rule check, Clock domain crossing check, layout verses schematic, layout techniques, verification, manufacturing tests		9
	UNIT III: Xilinx ISE, Actel libero, Active HDL, Quartus, Boole Dozer, Model Sim, design entries, various simulation, synthesis, place and route, timing verification		9
	UNIT IV: Cadence, IC station – design entries, simulations, various tools in the suit, GDS files. Microwind, Spice, Magic – layout techniques, simulations, DRCs		9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Course Code: VL 5254	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory Course		
Course Title & Code	Reconfigurable Computing (VL 5254)		
Course Objectives	● To understand the need and basics of reconfigurable architectures. ● To expose the students to HDL programming and develop applications with FPGAs.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the need and fundamentals of reconfigurable architectures	Knowledge/Comprehension (Level I/Level-II)
CO2	Point out the salient features of different reconfigurable architectures	Knowledge/Comprehension (Level I/Level-II)
CO3	Build basic modules using any HDL	Synthesis/Evaluation (Level-VI/Level-V)
CO4	Design and build an SOPC for a particular application	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**	**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	VHDL and Verilog (EC 3675)				

Text Books		
1.	Title	Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications
	Author	Christophe Bobda
	Publisher	Springer
	Edition	2010
Reference Books		
1.	Title	Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays
	Author	Maya B. Gokhale and Paul S. Graham
	Publisher	Springer
	Edition	2005
Course	**UNIT I:**	9

Contents	General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs– Device Architecture – Case Studies.	
	UNIT II: Compute Models – Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing	9
	UNIT III: Technology Mapping – FPGA Placement and Routing – Configuration Bit stream Generation – Case Studies with Appropriate Tools	9
	UNIT IV: Case Studies of FPGA Applications – System on a Programmable Chip (SOPC) Designs- Signal and image processing – Bioinformatics – Security – Special Topics – Partial Reconfiguration – Numerical Analysis - Performance Analysis/Prediction – Fault Tolerance	9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: EC 5255	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**Memory Technologies (VL 5255)**		
Course Objectives	• This course provides an in-depth exploration of semiconductor memory systems, ranging from traditional volatile memories to cutting-edge non-volatile technologies. • It covers the physics, circuit design, and architectural integration of memory arrays. Students will analyze the trade-offs between density, speed, power, and reliability, while exploring emerging technologies like MRAM, ReRAM, and 3D NAND that are driving the future of AI and high-performance computing.		

Course Outcomes		**Cognitive Levels**
CO1	Study the physical mechanisms and performance trade-offs between NAND and NOR flash architectures.	Knowledge/Comprehension (Level I/Level-II)
CO2	Analyze the stability and performance of SRAM/DRAM cells using industry-standard noise margin metrics.	Analysis (Level-IV)
CO3	Implement reliability strategies like ECC to mitigate hardware failures and soft errors in memory arrays	Application (Level-III)
CO4	Evaluate the potential of emerging NVMs (like STT-MRAM and ReRAM) to replace traditional storage in specific applications.	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**	**Winter**

Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	Low Power Devices and System (EC 4872), Low Power VLSI (EC 4755)				

Text Books		
1.	Title	Semiconductor Memories: Technology, Testing, and Reliability,
	Author	Ashok K. Sharma
	Publisher	Wiley-IEEE Press
	Edition	6th Edition
2.	Title	Emerging Memories: Technologies and Applications
	Author	Betty Prince
	Publisher	Cambridge University Press.
	Edition	6th ed.
Reference Books		
1.	Title	Digital Integrated Circuits: A Design Perspective
	Author	Jan M. Rabaey
	Publisher	Pearson
	Edition	5th edition

Course Contents		
	Unit 1: Volatile Memory Design (SRAM & DRAM) SRAM (Static RAM): 6T SRAM cell operation—read, write, and hold stability; Butterfly curves and Static Noise Margin (SNM), High-Speed SRAM: Peripheral circuits, sense amplifiers, and row/column decoders, DRAM (Dynamic RAM): 1T-1C cell architecture; Leakage mechanisms and refresh cycles, DRAM Scaling: Advanced capacitor structures (Trench and Stacked), and the architecture of DDR (Double Data Rate) interfaces.	**9**
	Unit 2: Traditional Non-Volatile Memory (NVM) ROM and PROM: Mask ROM, Floating gate physics, and EPROM/EEPROM; Flash Memory: NAND vs. NOR architectures; Programming and erasing mechanisms (Fowler-Nordheim tunneling and Hot Carrier Injection); Flash Reliability: Multi-Level Cell (MLC) and Triple-Level Cell (TLC) concepts; Wear leveling and endurance challenges; 3D NAND: Vertical string architecture and scaling limits.	**9**
	Unit 3: Emerging Next-Generation Memories Magnetoresistive RAM (MRAM): Magnetic Tunnel Junctions (MTJ) and Spin-Transfer Torque (STT-MRAM); Phase Change Memory (PCM): Chalcogenide materials, thermal switching, and amorphous-to-crystalline	**9**

	transitions; Resistive RAM (ReRAM): Filamentary vs. non-filamentary switching; Memristor theory; Ferroelectric RAM (FeRAM): Hysteresis loops and polarization-based storage.	
	Unit 4: Memory System Architecture & Testing Memory Hierarchy: Cache organization, tag/data arrays, and replacement policies; Error Correction: Hamming codes, ECC, and scrubbing techniques for soft errors; In-Memory Computing: Architecture for AI acceleration; Reducing the "Von Neumann Bottleneck; Testing & Yield: Built-in Self-Test (BIST) for memories; Fault models (Stuck-at, Coupling, and Neighborhood Pattern Sensitive Faults).	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5255	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	Y	N
Type of Course	Theory		
Course Title	**Filter Design (VL 5255)**		
Course Objectives	• To introduce the fundamental concepts of signals, noise, and advanced signal processing methods. • To understand transform-based and statistical model-based signal processing techniques for noise reduction. • To study linear prediction models, eigenvalue analysis, PCA, and power spectrum estimation methods. • To understand impulse noise modeling, detection, and removal techniques using signal processing approaches.		

Course Outcomes		**Cognitive Levels**
CO1	Understand the basic concepts of signals, noise, information, and modern signal processing techniques.	Knowledge/Comprehension (Level-I/Level-II)
CO2	Analyze different classes of noise and signal distortion using transform-based and Bayesian statistical signal processing methods.	Analysis (Level-IV)
CO3	Apply linear prediction models, eigenvalue decomposition, PCA, and spectral estimation techniques for signal analysis.	Application (Level-III)
CO4	Evaluate impulse noise models and implement suitable detection and removal techniques using linear prediction methods.	Evaluation/Synthesis (Level-V/Level-VI)

Semester	**II**	**Winter**			
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course	Signals and Systems				

codes with course names	Digital Signal Processing Probability and Random Processes		
Text Books			
1.	Title	Advanced Signal Processing and Noise Reduction	
	Author	S. V. Vaseghi	
	Publisher	Wiley	
	Edition	4th Edition, 2008	
Reference Books			
1.	Title	Statistical Digital Signal Processing and Modeling	
	Author	Monson H. Hayes	
	Publisher	Wiley	
	Edition	1996	
2.	Title	Digital Signal Processing: Principles, Algorithms and Applications	
	Author	Proakis and Manolakis	
	Publisher	Pearson	
	Edition	4th Edition	
3.	Title	Adaptive Filter Theory	
	Author	Simon Haykin	
	Publisher	Pearson	
	Edition	5th Edition	
Course Contents	**UNIT I: Signals, Noise and Signal Processing Fundamentals** Signals, noise, and information; deterministic and random signals; signal representation and characterization; signal processing methods; transform-based signal processing techniques; Fourier transform, short-time Fourier transform, wavelet transform; source-filter model-based signal processing concepts and applications.		**9**
	UNIT II: Noise Modeling and Statistical Signal Processing Different classes of noise and distortion; white noise, colored noise, Gaussian noise, impulse noise; Bayesian statistical model-based signal processing; statistical estimation concepts; noise suppression and filtering techniques; adaptive filtering basics; transform-domain noise reduction methods.		**9**
	UNIT III: Linear Prediction Models and Spectral Analysis Linear prediction models; forward and backward linear prediction; autoregressive (AR) modeling; eigenvalue analysis and principal component analysis (PCA); covariance and correlation matrices; power spectrum analysis; spectral estimation techniques and applications in signal processing.		**9**
	UNIT IV: Impulse Noise Modeling and Removal Techniques Impulse noise modeling and characteristics; impulse noise detection techniques; impulse noise removal methods; median filtering and adaptive filtering approaches; impulse noise suppression using linear prediction models; performance analysis and applications in speech, image, and communication signal processing.		**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%	

Course Code: VL 5255	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory Course		
Course Title & Code	CPLD & FPGA Architecture (VL5255)		
Course Objectives	● To understand the various Programmable Logic Devices. ● To design and implement various digital circuits using FPGA and CPLD.		

Course Outcomes		**Cognitive Levels**
CO1	Learn and understand the knowledge of PLDs, FPGA Design and architecture.	Knowledge/Comprehension (Level I/Level-II)
CO2	Understand the different types of arrays	Application (Level-III)
CO3	Design and analyse the FSM techniques and different case studies	Analysis (Level-IV)
CO4	Test and implement various digital circuits using FPGA and CPLD	Synthesis/Evaluation (Level-VI/Level-V)

Semester	**II**	**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	Digital Electronics (EC 2401)				

Text Books		
1.	Title	Field Programmable Gate Array Technology
	Author	Stephen M. Trimberger
	Publisher	Springer
	Edition	
2.	Title	Field Programmable Gate Arrays
	Author	John V. Oldfield, Richard C. Dorf
	Publisher	Wiley
	Edition	

Reference Books		
1.	Title	Digital Design Using Field Programmable Gate Arrays
	Author	-Pak K. Chan/Samiha Mourad
	Publisher	Pearson
	Edition	

Course Contents	**UNIT I:** Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic;	9
	UNIT II: Complex Programmable Logic Devices –Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation. Organization of FPGAs,	9
	UNIT III: FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs	9
	UNIT IV: The Xilinx XC2000, XC3000 and XC4000 Architectures. Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.	9
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%

Course Code: VL 5256	**Open Elective Course: (Y/N)**	**Departmental Core Course: (Y/N)**	**Departmental Elective Course: (Y/N)**
	N	N	Y
Type of Course	Theory		
Course Title	**System on Chip (SoC) (EC 5254)**		
Course Objectives	• To provide knowledge of modern System-on-Chip (SoC) technologies, CMOS design principles, and VLSI implementation methodologies. • To understand hardware/software co-design techniques and optimization strategies for SoC implementation. • To study timing, power, interconnect, memory, and data path optimization techniques in integrated system design. • To introduce floor planning, routing, clock distribution, verification, and complete chip design methodologies.		

Course Outcomes		**Cognitive Levels**
CO1	Understand CMOS technology, SoC design methodologies, IC economics, hierarchical design concepts, and EDA tool flow for modern SoC implementation.	Knowledge/Comprehension (Level-I/Level-II)
CO2	Apply hardware/software co-design concepts and implement optimized hardware and software solutions for SoC systems.	Application (Level-III)
CO3	Analyze timing, power, datapath, interconnect, and memory architectures to optimize SoC performance under implementation constraints.	Analysis (Level-IV)
CO4	Evaluate complete SoC design methodologies including floor	Evaluation/Synthesis

	planning, routing, verification, IP reuse, testing, and chip-level implementation challenges.	(Level-V/Level-VI)

Semester	**II**		**Winter**		
Contact Hours	**Lecture**	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
	3	0	0	3	36
Prerequisite course codes with course names	Digital VLSI Design CMOS VLSI Design Computer Architecture Embedded Systems				

Text Books			
1.	Title	Modern VLSI Design	
	Author	Wayne Wolf	
	Publisher	Pearson Education	
	Edition	1998	
2.	Title	Principles of CMOS VLSI Design	
	Author	Kamran Eshraghian	
	Publisher	Pearson Education	
	Edition	2007	
3.	Title	Digital Integrated Circuit Design	
	Author	Jan M. Rabaey and Anantha Chandrakasan	
	Publisher	Pearson Education	
	Edition	2009	
Reference Books			
1.	Title	CMOS Digital Integrated Circuits	
	Author	Sung-Mo Kang and Yusuf Leblebici	
	Publisher	McGraw Hill	
	Edition	4th Edition	
2.	Title	System-on-Chip Design	
	Author	Michael J. Flynn and Wayne Luk	
	Publisher	Oxford University Press	
	Edition	2011	
3.	Title	CMOS Circuit Design, Layout and Simulation	
	Author	R. Jacob Baker	
	Publisher	Wiley	
	Edition	3rd Edition	

Course Contents	**UNIT I: SoC Design Fundamentals and CMOS Technology** Introduction to System-on-Chip (SoC); IC technology and economics; CMOS technology overview; power consumption in CMOS circuits; hierarchical design methodology; design abstraction levels; EDA tools and design flow; MOSFET models; transistor parasitic; latch-up effects; advanced transistor structures; wire parasitic; scalable design rules and process parameters.	**9**
	UNIT II: Hardware/Software Co-Design and Layout Design Hardware/software partitioning and co-design methodologies; hardware/software trade-offs; stick diagrams and layout design tools; layout synthesis and layout analysis; CMOS gate delays; transmission time; speed-power product; low-power logic gates; implementation of switch logic	**9**

	networks; logic and interconnect design strategies.	
	UNIT III: Datapath Design, Timing and Power Optimization Delay modelling using RC and RLC networks; crosstalk effects; wire sizing techniques; pipelining and data path architectures; adders, ALUs, multipliers, and high-density memory structures; metastability and multiphase clocking; low-power architecture design; power optimization techniques; sequential testing and design validation methodologies.	**9**
	UNIT IV: Physical Design, Verification and Complete SoC Design Floor planning methods; global routing and switch-box routing; clock distribution techniques; off-chip connections and packaging technologies; I/O architectures and pad design; intellectual property (IP) reuse and verification challenges; SoC integration and testing; complete chip design methodology including architecture, logic, and layout design for applications such as kitchen timer chip or microwave oven chip.	**9**
Course Assessment	Total Marks=100	Continuous Evaluation 20% Mid Semester 30% End Semester 50%